IOb-SoC: IObundle System-on-Chip

Pedro Miranda

IObundle, Lda.

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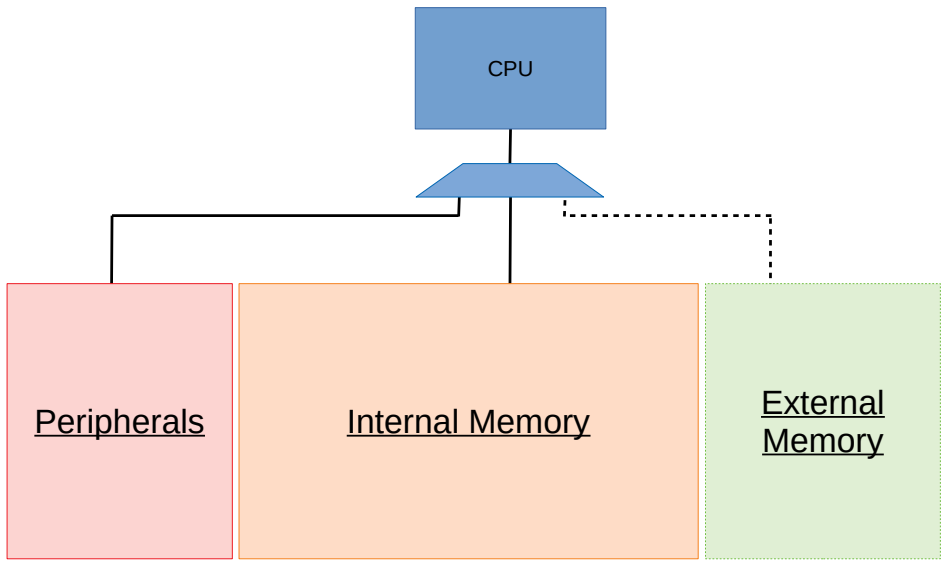
IOb-SoC Hardware Platform

Open source RISC-V SoC platform by IObundle.

Main components:

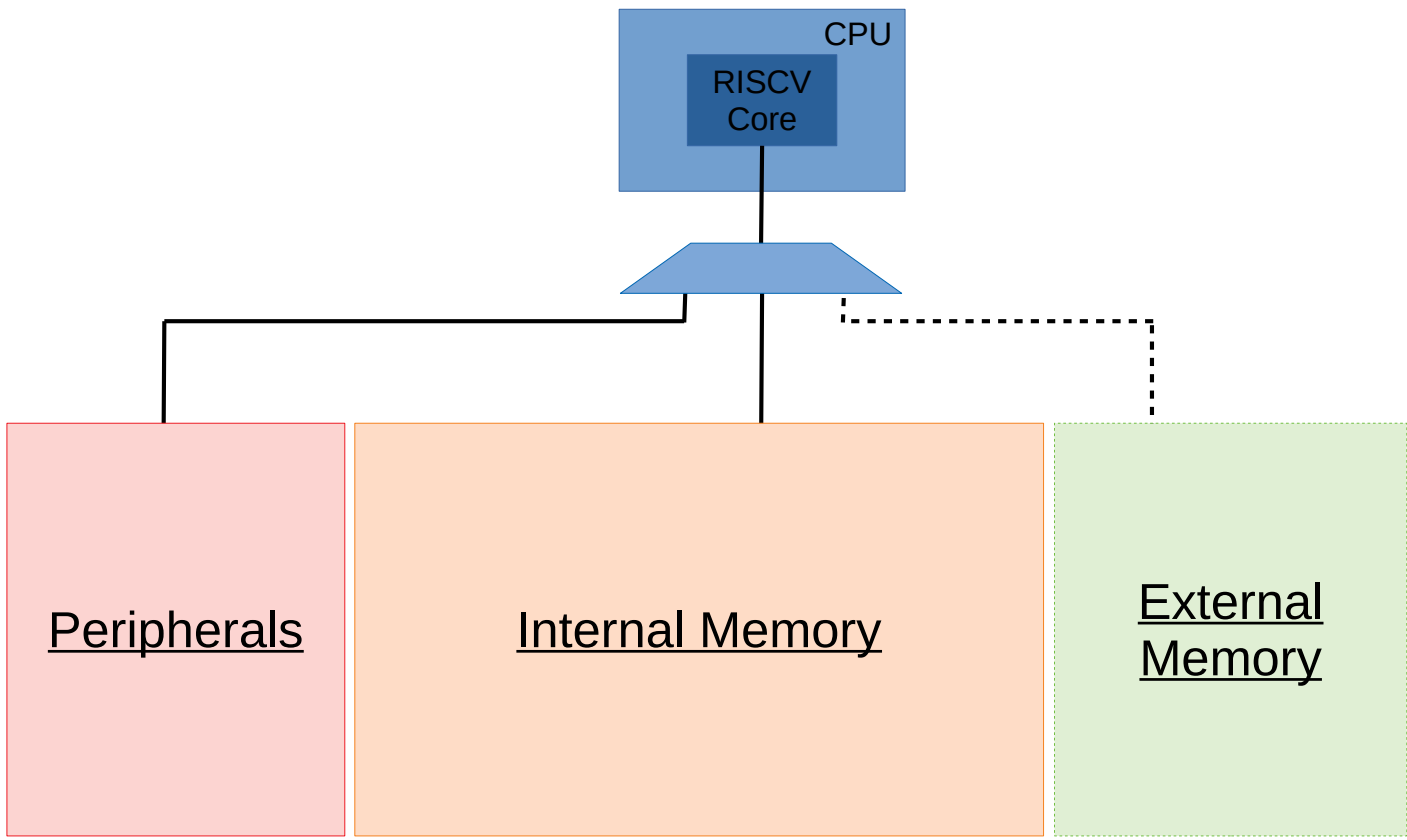
- RISC-V CPU
- Internal memory
- External memory
  - Cache
- Integrated Peripherals



Continuous integration of system and new components.
Development of testing environment.

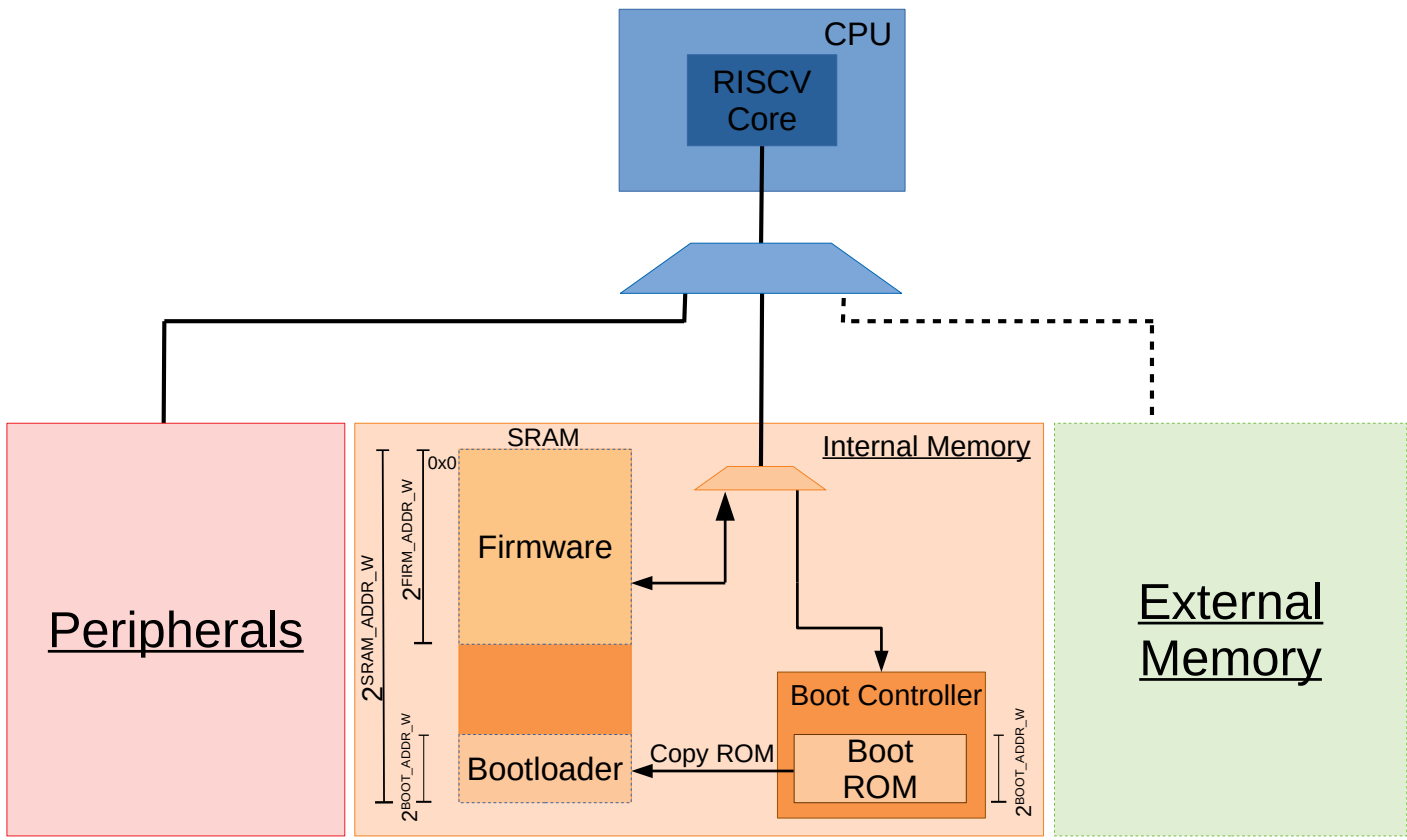
IOb-SoC Architecture: CPU

- RISCV Core
  - PicoRV
  - DarkRV
  - SSRV
- CPU Wrapper
  - Interface with System



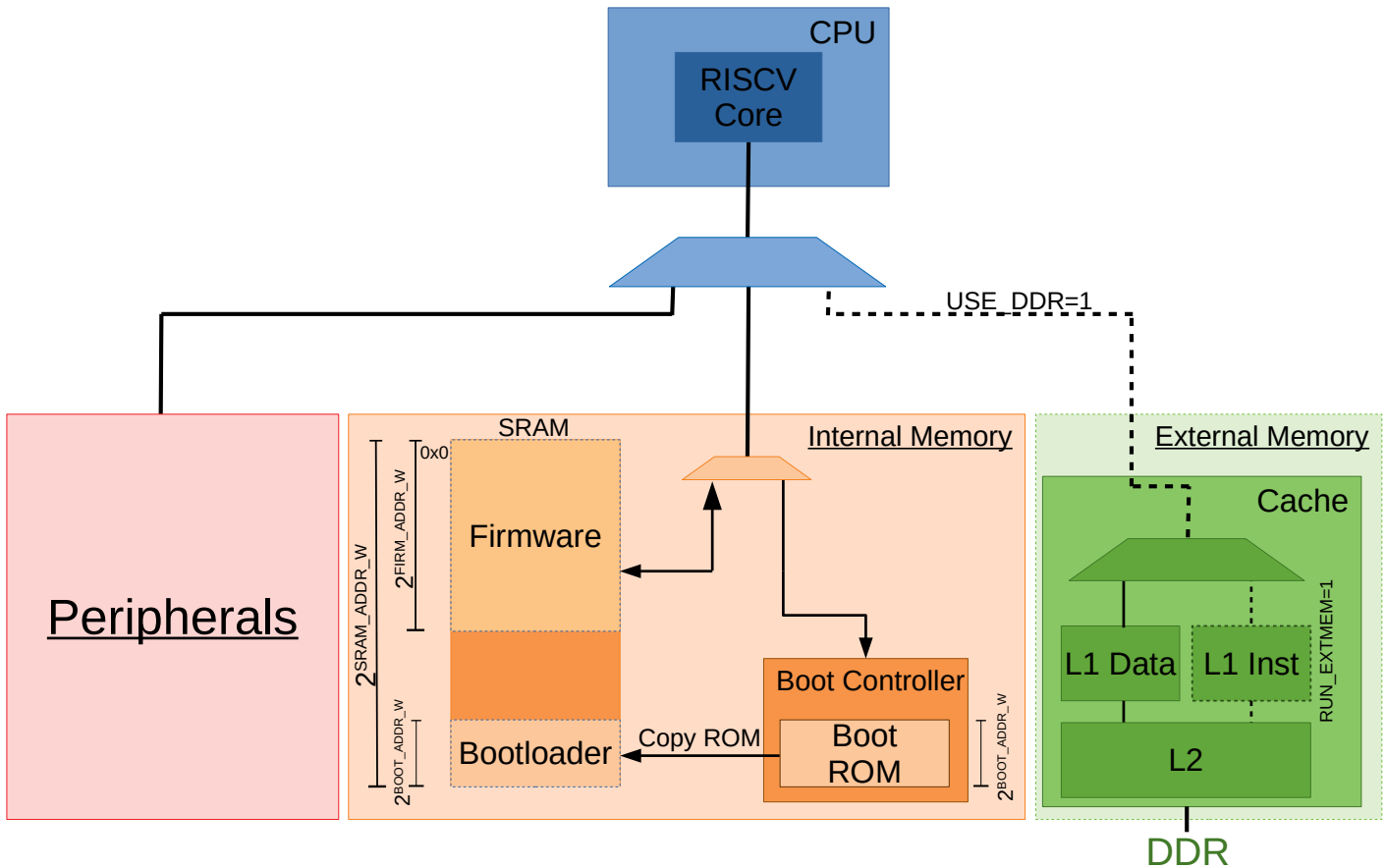
IOb-SoC Architecture: Internal Memory

- Static RAM (SRAM)
  - Small Firmwares
  - Scratchpad Memory
- Boot Controller
  - ROM with Bootloader Program
  - Write to SRAM on Reset



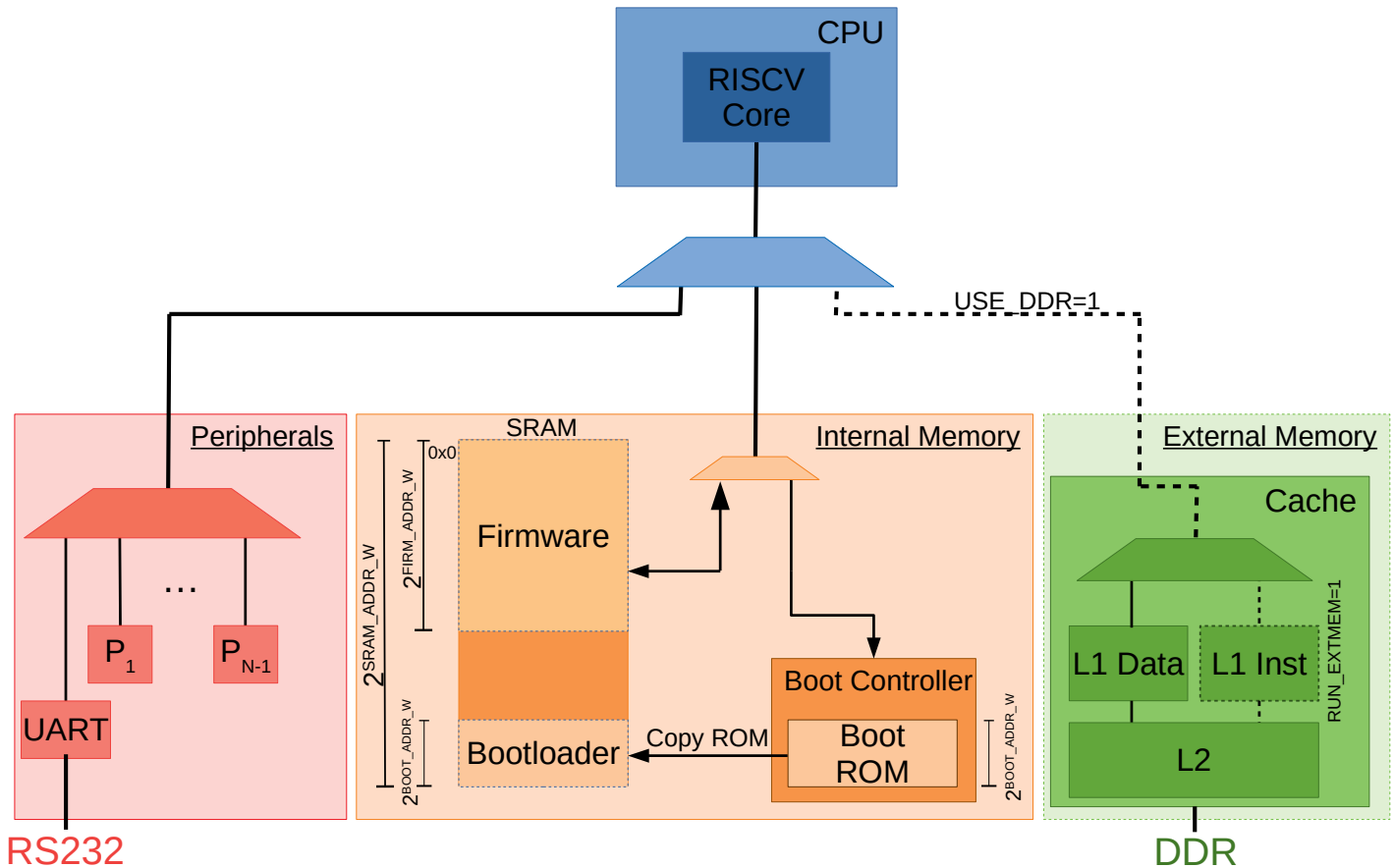
IOb-SoC Architecture: External Memory

- L2 Cache
  - AXI4 Full (DDR side)
  - Native Interface (CPU side)
  - Configurable Bus Width
- L1 Cache
  - Data Cache
  - Instruction Cache



IOb-SoC Architecture: Peripherals

- UART
  - Data file transfer
  - Program Firmware
  - Debug Messages
- Other Peripherals
  - Communication (Ethernet, I2S, I^2C)
  - Specialized Accelerators
  - IP Core in Development



Check out **IOb-SoC** at:

`github.com/IObundle/iob-soc`