PEPCC

G01.Project Summary

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PEPCC

Project Details

Planned Start Date: 1st of October, 2018 → **Effective End Date: 31st of December 2021**

Planned Duration: 2.5 years

Project Reference: PTDC/EEI-HAC/30848/2017

Call: 02/SAICT/2017

Funded Under: FCT (Fundação para a Ciência e a Tecnologia)

Total Funding: 239.591,66€

Power Efficiency and Performance for Embedded and HPC Systems with Custom CGRAs

https://pepcc.inesctec.pt/

Papers

Year	Venue	Title
2019	IEEE TVLSI	Dynamic Partial Reconfiguration of Customized Single-Row Accelerators
2019	IEEE ISCAS	Low Energy Heterogeneous Computing with Multiple RISC-V and CGRA Cores
2020	ACM CSUR	Improving Performance and Energy Consumption in Embedded Systems via Binary Acceleration: A Survey
2020	DATE 2020	Project Poster + Binary Translation Framework Demo
2020	IEEE Access	Optimizing OpenCL Code for Performance on FPGA: k-means Case Study with Integer Data Sets
2020	FPL 2020	Executing ARMv8 Loop Traces on Reconfigurable Accelerator via Binary Translation Framework
2020	ARC 2020	Implementing CNNs Using a Linear Array of Full Mesh CGRAs
2021	MDPI Electronics	Transparent Control Flow Transfer between CPU and Accelerators for HPC
2021	ASPLOS 2021 (LATTE)	A Position on Transparent Reconfigurable Systems
2021	IEEE Access	A Full Featured Configurable Accelerator for Object Detection with YOLO
2021	IEEE Micro	A Binary Translation Framework for Automated Hardware Generation
2021	MDPI Electronics	Coarse-Grained Reconfigurable Computing with the Versat Architecture
2021	FPT 2021	On the Performance Effect of Loop Trace Window Size on Scheduling for Configurable Coarse Grain Loop Accelerators
2021	MDPI Algorithms	IOb-Cache: A High-Performance Configurable Open-Source Cache
2021	MDPI Future Internet	Configurable Hardware Core for IoT Object Detection
2022	ISCAS (submitted)	A Flexible HLS Hoeffding Tree Implementation for Runtime Learning on FPGA

Artifacts

- Repositories
  - ***specs-hw***, *“Binary Translation Tools”*
  - ***specs-chisel***, *“Chisel-based Hardware Architectures”*
  - ***iob-soc,*** *“Multicore RISC-V SoC + Versat CGRA Template”*
- Media
  - Interactive Web-Demo for Binary Translation Framework!
  - Video Demo at FPL 2020
  - Video Demo at DATE 2020

- Scientific/Technical
  - *“A Generator of Randomly Correlated N-Dimentional Clusters” @RG*
  - *“A Batch of Integer Data Sets for Clustering Algorithms” @IEEE Dataport*
  - *“A Test Harness for Multiple OpenCL Implementations of the k-means Algorithm“ @CodeOcean*
  - *“A Dataset for Desktop Processor Characteristics from 1970 to 2019” @RG*

Programme

Hora	Título	Orador
14:00	Project Summary	JCF/JS
14:05	DPR of Loop Accelerators (IEEE VLSI)	NP
14:15	k-means em FPGA via OpenCL (IEEE Access)	NP
14:25	An Overview on Binary Translation (ACM CSUR)	NP
14:35	Versat (MDPI Electronics)	JTS
14:45	Yolo (IEEE Access)	JTS
14:55	INESC ID #3 (TBD)	TDB
15:05	Discussion Break #1	-
15:10	Introducing the Binary Translation Framework (IEEE Micro, FPL2020, and DATE2020)	NP
15:20	BTF. Binary Parsing	NP
15:25	BTF. Visualizing Trace Graphs / Segment Detection and CDFGs	NP
15:30	BTF. Dataflow Graphs and Analysis Steps; AGU Generation	TS
15:40	CrispyHDL	NP
15:45	Discussion Break #2	-
15:50	Versat Architecture	J. Lopes
16:00	Versat Compiler	R. Teixeira
16:10	RNN on Versat	B. Joudat
16:15	IOb-SoC	P. Miranda
16:20	Discussion Break #3	-
16:25	Retrospectiva / Dificuldades	Todos
16:35	Direcções Futuras (Científicas e Financiamento)	Todos
16:45	Fecho	JCF/JS